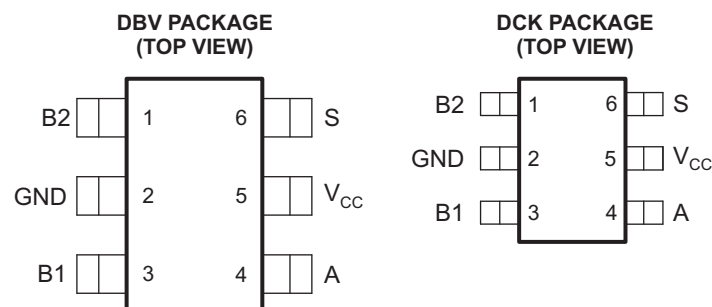


SINGLE-POLE DOUBLE-THROW ANALOG SWITCH

FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 1.65-V to 5.5-V V_{CC} Operation
- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity
- High Speed, Typically 0.5 ns ($V_{CC} = 3\text{ V}$, $C_L = 50\text{ pF}$)
- Low On-State Resistance, Typically $\approx 6\ \Omega$ ($V_{CC} = 4.5\text{ V}$)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-pole double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G3157 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOT (SOT-23) – DBV	Reel of 3000	1P1G3157QDBVRQ1	CC50
	SOT (SC-70) – DCK	Reel of 3000	1P1G3157QDCKRQ1	C50

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

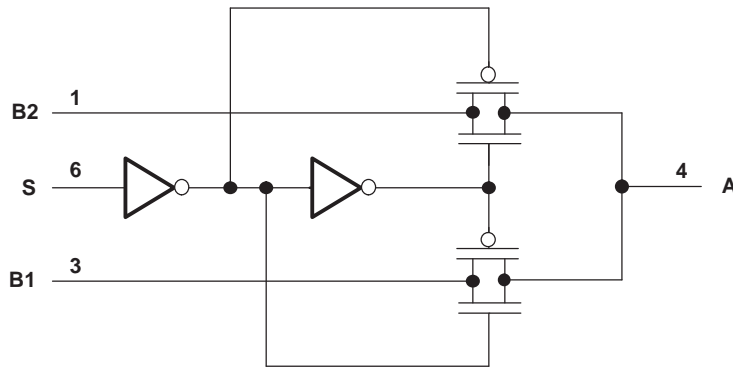
FUNCTION TABLE

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.5	6.5	V
V _{IN}	Control input voltage range ⁽²⁾⁽³⁾	-0.5	6.5	V
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Control input clamp current	V _{IN} < 0		-50 mA
I _{IOK}	I/O port diode current	V _{I/O} < 0		-50 mA
I _{I/O}	On-state switch current	V _{I/O} = 0 to V _{CC} ⁽⁶⁾		±128 mA
Continuous current through V _{CC} or GND				±100 mA
θ _{JA}	Package thermal impedance ⁽⁷⁾	DBV package		165 °C/W
		DCK package		258 °C/W
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for V_{I/O}.
- (6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for I_{I/O}.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}			1.65	5.5	V
$V_{I/O}$			0	V_{CC}	V
V_{IN}			0	5.5	V
V_{IH}	High-level input voltage, control input	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$V_{CC} \times 0.75$		V
		$V_{CC} = 2.3\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control input	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$V_{CC} \times 0.25$		V
		$V_{CC} = 2.3\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$		
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	20		ns/V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	20		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	10		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	10		
T_A			-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
r _{on}	On-state switch resistance ⁽²⁾	See Figure 1 and Figure 2	V _I = 0 V, I _O = 4 mA	1.65 V		11	20	Ω	
			V _I = 1.65 V, I _O = –4 mA			15	50		
			V _I = 0 V, I _O = 8 mA	2.3 V		8	12		
			V _I = 2.3 V, I _O = –8 mA			11	30		
			V _I = 0 V, I _O = 24 mA	3 V		7	9.5		
			V _I = 3 V, I _O = –24 mA			9	20		
			V _I = 0 V, I _O = 30 mA	4.5 V		6	7.5		
			V _I = 2.4 V, I _O = –30 mA			7	12		
			V _I = 4.5 V, I _O = –30 mA			7	15		
r _{range}	On-state switch resistance over signal range ⁽²⁾⁽³⁾	0 ≤ V _{Bn} ≤ V _{CC} (see Figure 1 and Figure 2)	I _A = –4 mA	1.65 V			140	Ω	
			I _A = –8 mA	2.3 V			45		
			I _A = –24 mA	3 V			18		
			I _A = –30 mA	4.5 V			10		
Δr _{on}	Difference in on-state resistance between switches ⁽²⁾⁽⁴⁾⁽⁵⁾	See Figure 1	V _{Bn} = 1.15 V, I _A = –4 mA	1.65 V		0.5	Ω		
			V _{Bn} = 1.6 V, I _A = –8 mA	2.3 V		0.1			
			V _{Bn} = 2.1 V, I _A = –24 mA	3 V		0.1			
			V _{Bn} = 3.15 V, I _A = –30 mA	4.5 V		0.1			
r _{on(flat)}	On-state resistance flatness ⁽²⁾⁽⁴⁾⁽⁶⁾	0 ≤ V _{Bn} ≤ V _{CC}	I _A = –4 mA	1.65 V		110	Ω		
			I _A = –8 mA	2.3 V		26			
			I _A = –24 mA	3 V		9			
			I _A = –30 mA	4.5 V		4			
I _{off} ⁽⁷⁾	Off-state switch leakage current	0 ≤ V _I , V _O ≤ V _{CC} (see Figure 3)	1.65 V to 5.5 V			±1 ±0.05	±1 ⁽¹⁾	μA	
I _{S(on)}	On-state switch leakage current	V _I = V _{CC} or GND, V _O = Open (see Figure 4)	5.5 V			±1 ±0.1 ⁽¹⁾		μA	
I _{IN}	Control input current	0 ≤ V _{IN} ≤ V _{CC}	0 V to 5.5 V			±1 ±0.05	±1 ⁽¹⁾	μA	
I _{CC}	Supply current	V _{IN} = V _{CC} or GND	5.5 V		1	10		μA	
ΔI _{CC}	Supply-current change	V _{IN} = V _{CC} – 0.6 V	5.5 V			500		μA	
C _{in}	Control input capacitance	S	5 V		2.7			pF	
C _{io(off)}	Switch input/output capacitance	Bn	5 V		5.2			pF	
C _{io(on)}	Switch input/output capacitance	Bn	5 V		17.3			pF	
		A		17.3					

(1) T_A = 25°C

(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. On-state resistance is determined by the lower of the voltages on the two (A or B) ports.

(3) Specified by design

(4) Δr_{on} = r_{on(max)} – r_{on(min)} measured at identical V_{CC}, temperature, and voltage levels

(5) This parameter is characterized, but not tested in production.

(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.

(7) I_{off} is the same as I_{S(off)} (off-state switch leakage current).

Analog Switch Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch on) ⁽¹⁾	A or Bn	Bn or A	$R_L = 50 \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6)	1.65 V	300	MHz
				2.3 V	300	
				3 V	300	
				4.5 V	300	
Crosstalk (between switches) ⁽²⁾	B1 or B2	B2 or B1	$R_L = 50 \Omega$, $f_{in} = 10 \text{ MHz}$ (sine wave) (see Figure 7)	1.65 V	-54	dB
				2.3 V	-54	
				3 V	-54	
				4.5 V	-54	
Feedthrough attenuation (switch off) ⁽²⁾	A or Bn	Bn or A	$C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, $f_{in} = 10 \text{ MHz}$ (sine wave) (see Figure 8)	1.65 V	-57	dB
				2.3 V	-57	
				3 V	-57	
				4.5 V	-57	
Charge injection ⁽³⁾	S	A	$C_L = 0.1 \text{ nF}$, $R_L = 1 \text{ M}\Omega$ (see Figure 9)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	$V_I = 0.5 \text{ V}_{p-p}$, $R_L = 600 \Omega$, $f_{in} = 600 \text{ Hz to } 20 \text{ kHz}$ (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

(3) Specified by design

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5 and Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} ⁽¹⁾	A or Bn	Bn or A	2		1.2		0.8		0.3		ns
t_{en} ⁽²⁾	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t_{dis} ⁽³⁾			3	13	2	7.5	1.5	5.3	0.8	3.8	
t_{B-M} ⁽⁴⁾			0.5		0.5		0.5		0.5		ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL} . Propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

(2) t_{en} is the slower of t_{PZL} or t_{PZH} .

(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ} .

(4) Specified by design

PARAMETER MEASUREMENT INFORMATION

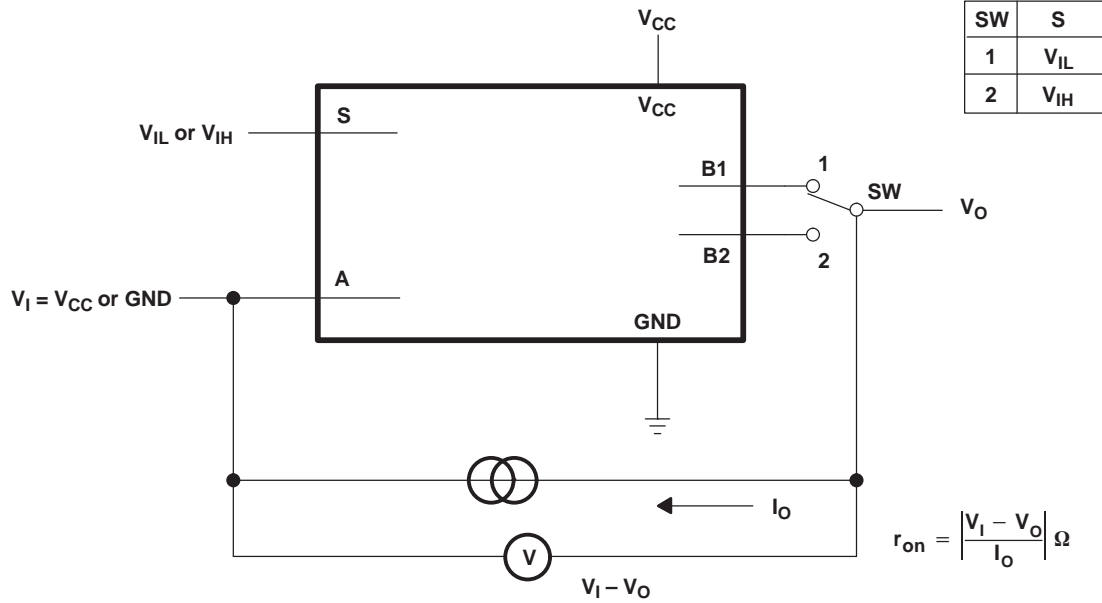


Figure 1. On-State Resistance Test Circuit

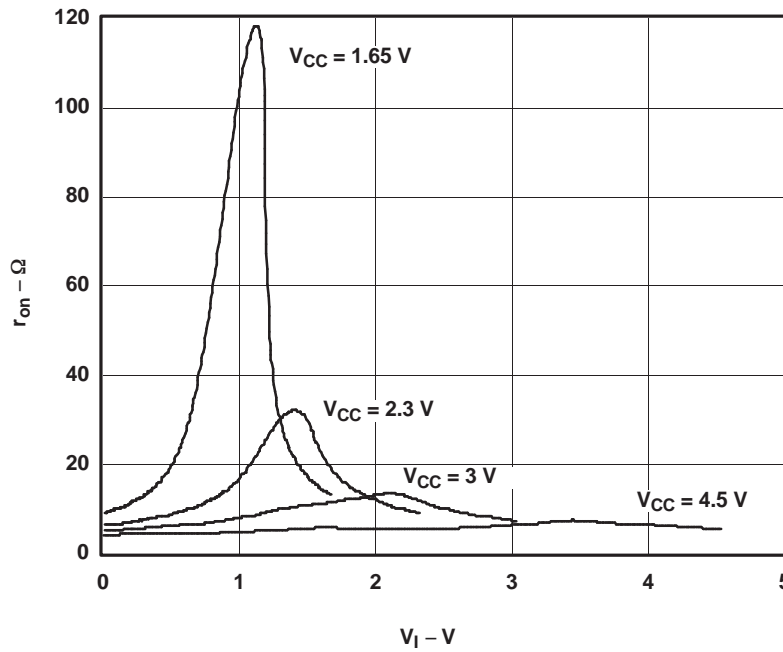
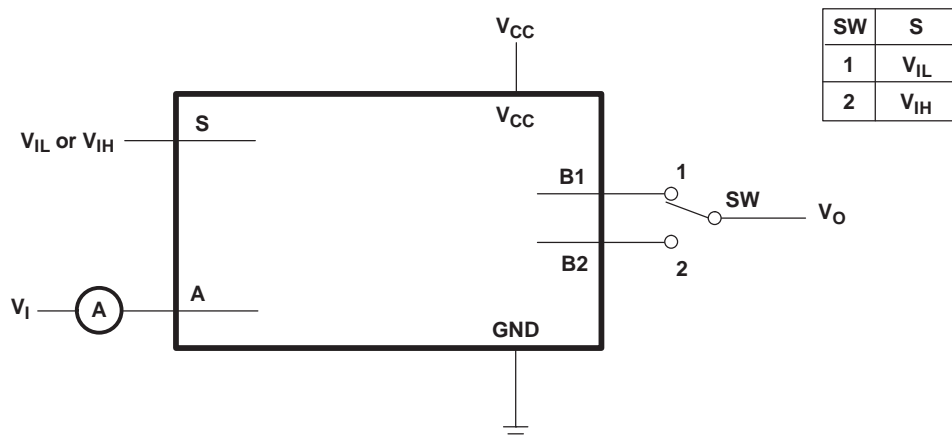


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION (continued)



Condition 1: $V_I = \text{GND}$, $V_O = V_{CC}$
 Condition 2: $V_I = V_{CC}$, $V_O = \text{GND}$

Figure 3. Off-State Switch Leakage-Current Test Circuit

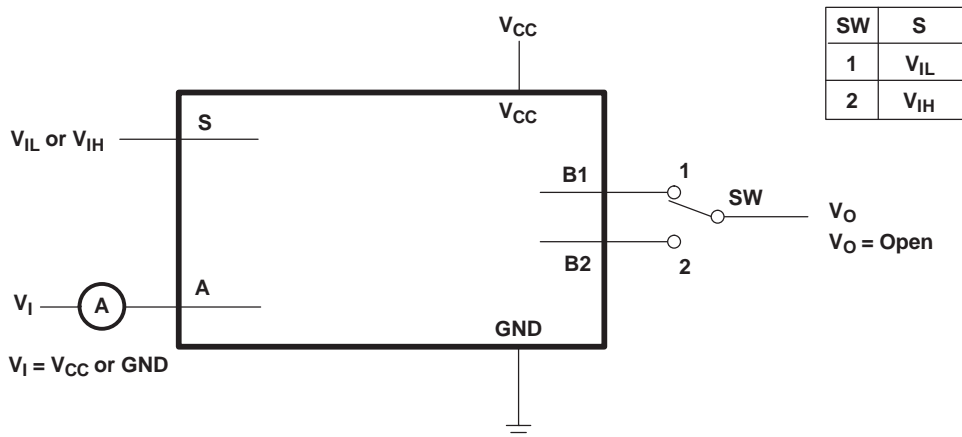
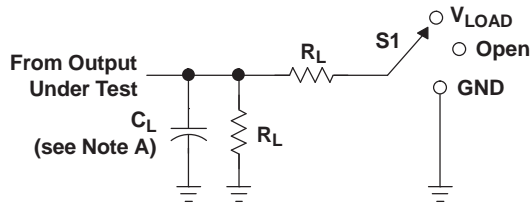


Figure 4. On-State Switch Leakage-Current Test Circuit

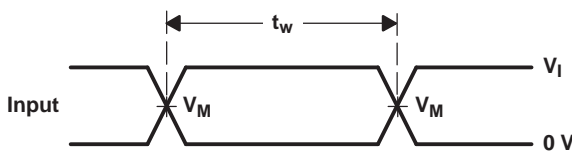
PARAMETER MEASUREMENT INFORMATION (continued)



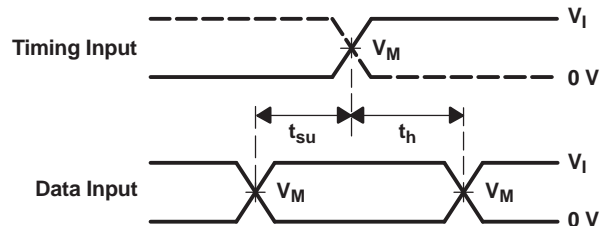
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

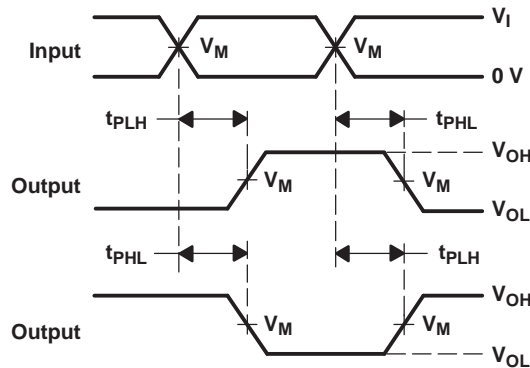
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



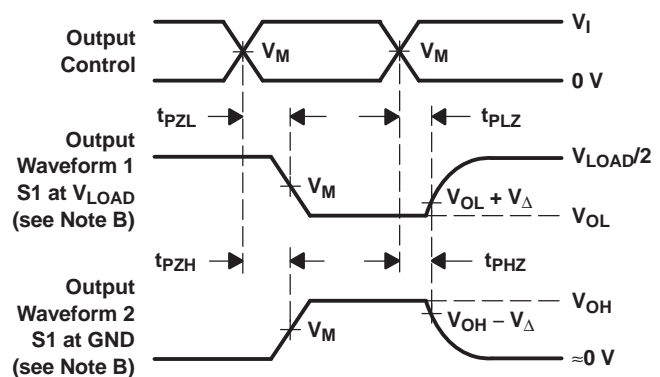
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

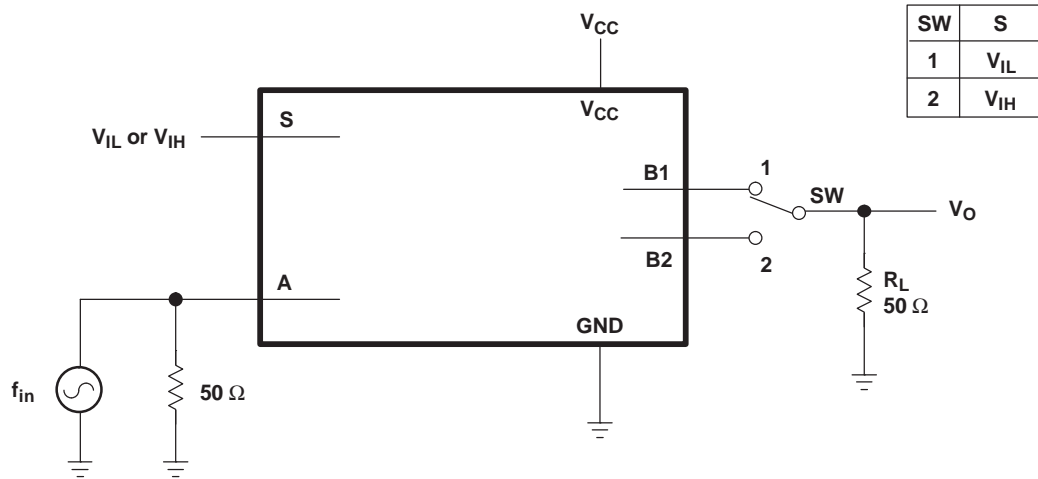


Figure 6. Frequency Response (Switch On)

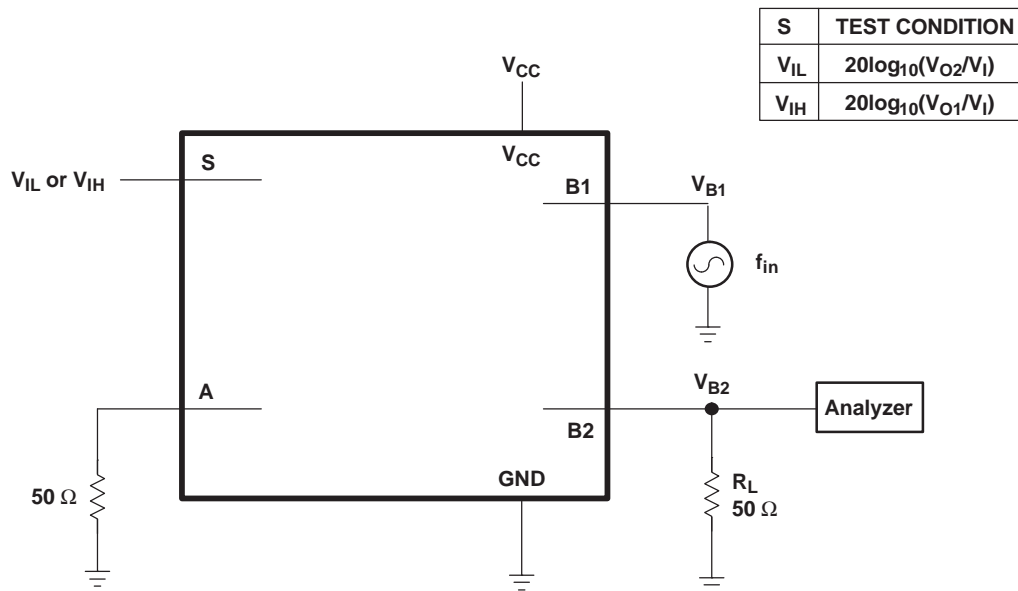


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION (continued)

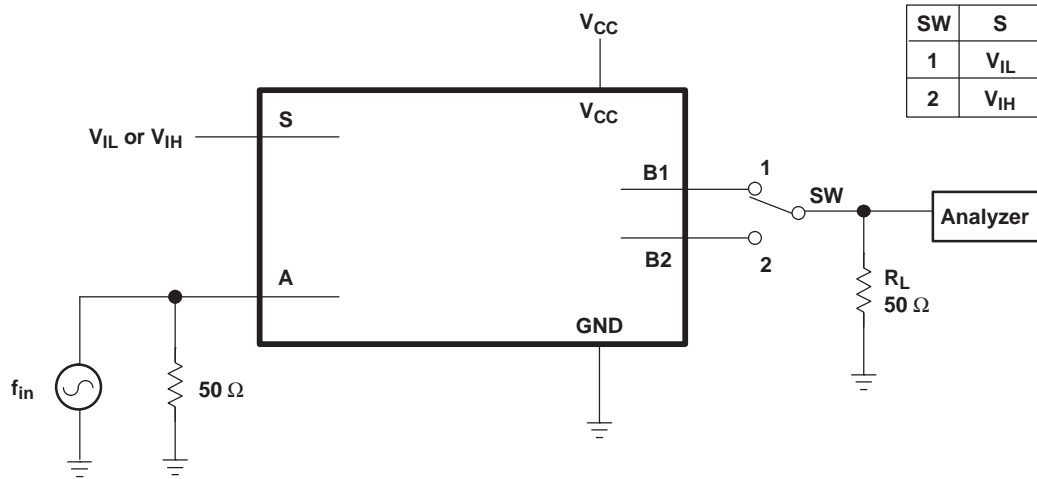


Figure 8. Feedthrough

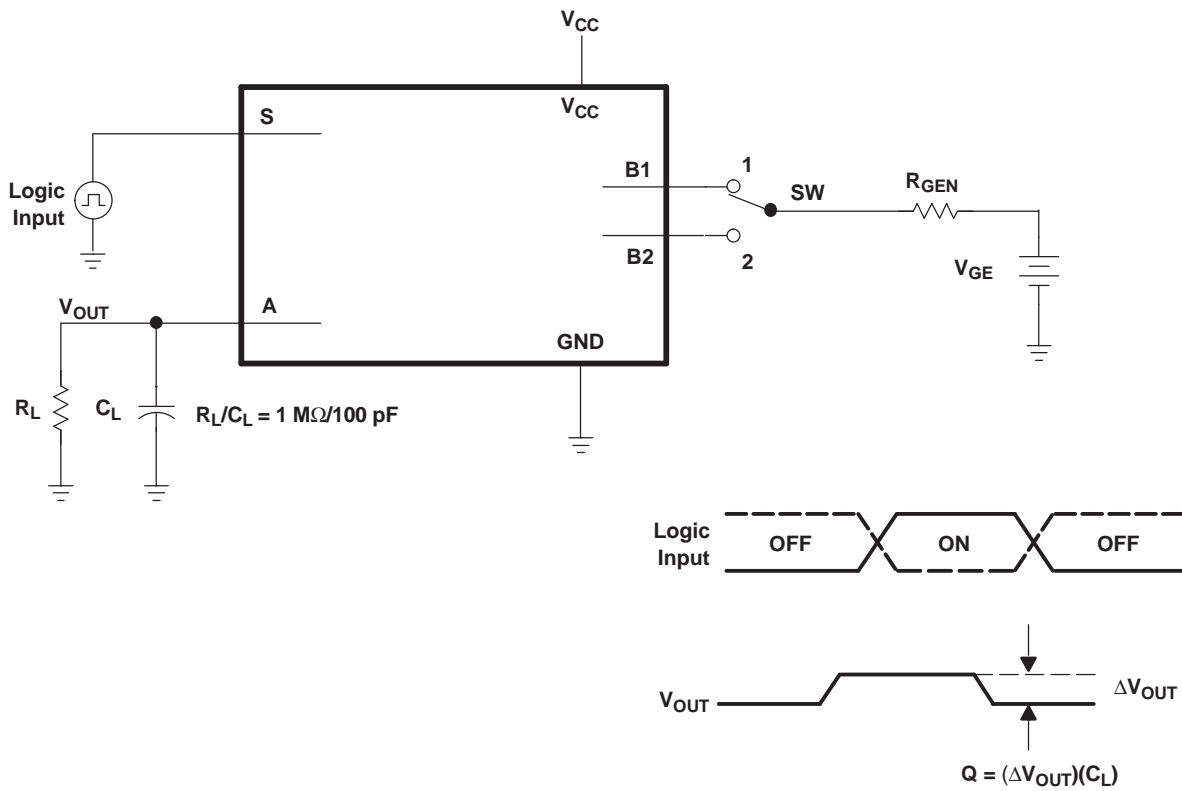


Figure 9. Charge-Injection Test

PARAMETER MEASUREMENT INFORMATION (continued)

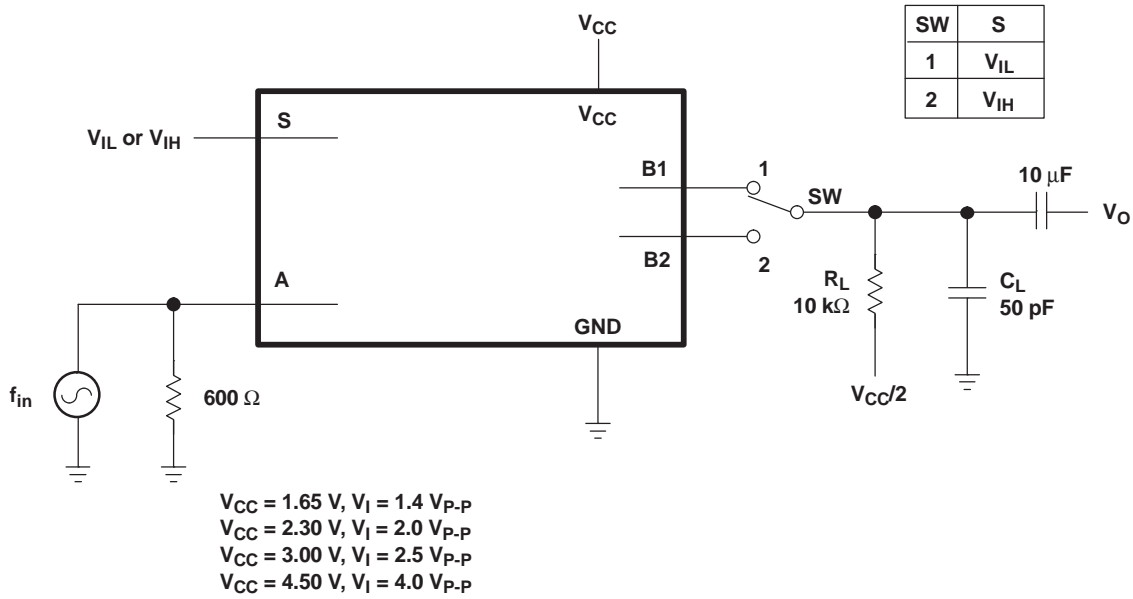


Figure 10. Total Harmonic Distortion

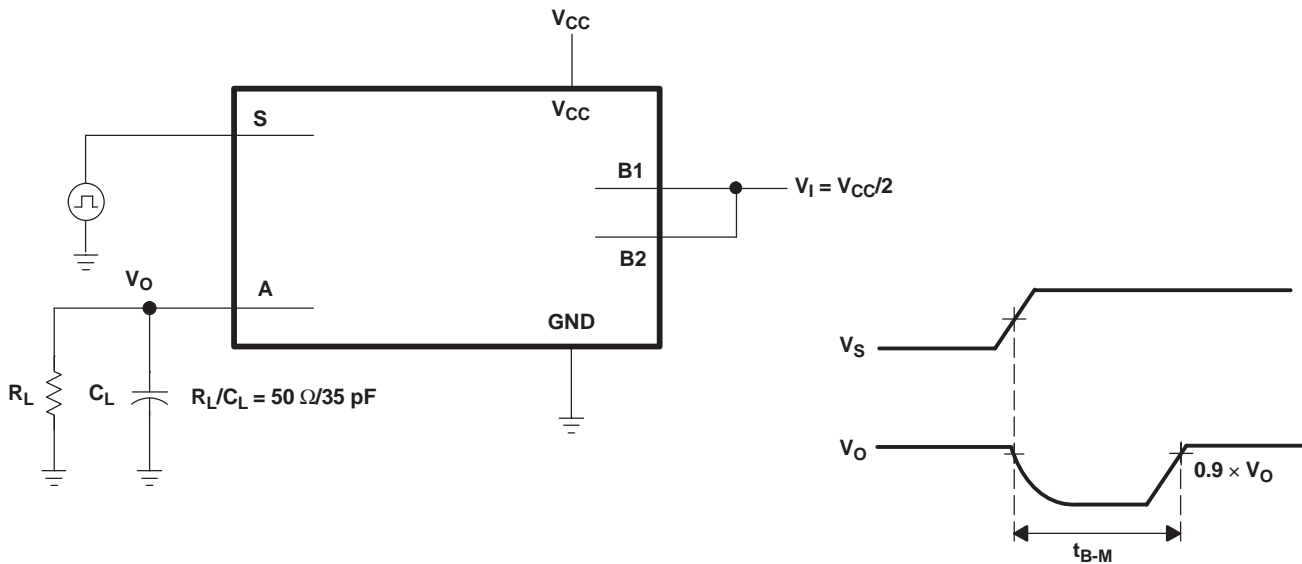


Figure 11. Break-Before-Make Internal Timing

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
1P1G3157QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
1P1G3157QDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G3157-Q1 :

- Catalog: [SN74LVC1G3157](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- \triangle Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

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